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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,311	03/24/2004	Atsushi Yoshimura	04329.3292	3790
22852	7590	11/29/2005	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			DIAZ, JOSE R	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. <u>10/807,311</u>	Applicant(s) YOSHIMURA, ATSUSHI	
	Examiner José R. Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 13 September 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) 1-8, 17 and 18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

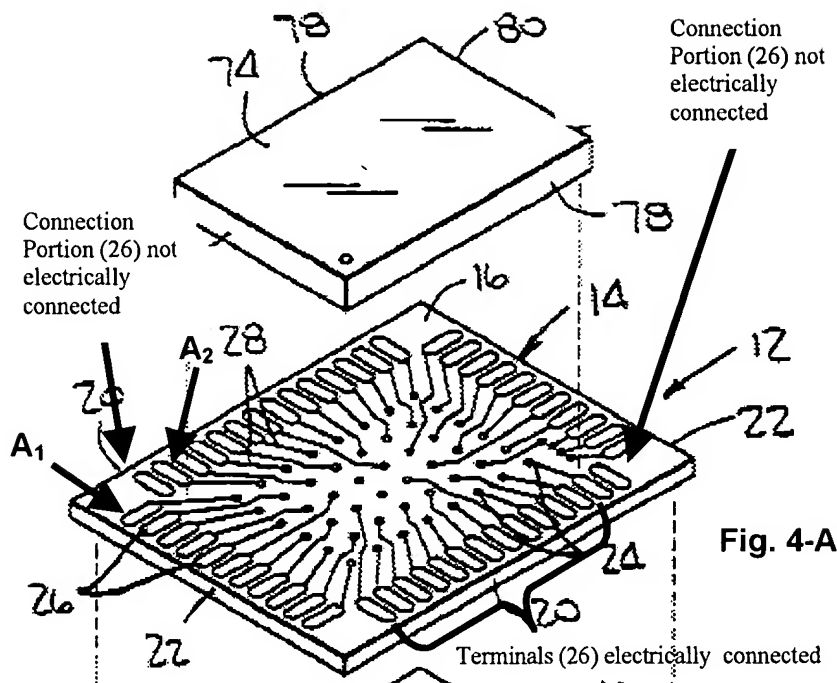
A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

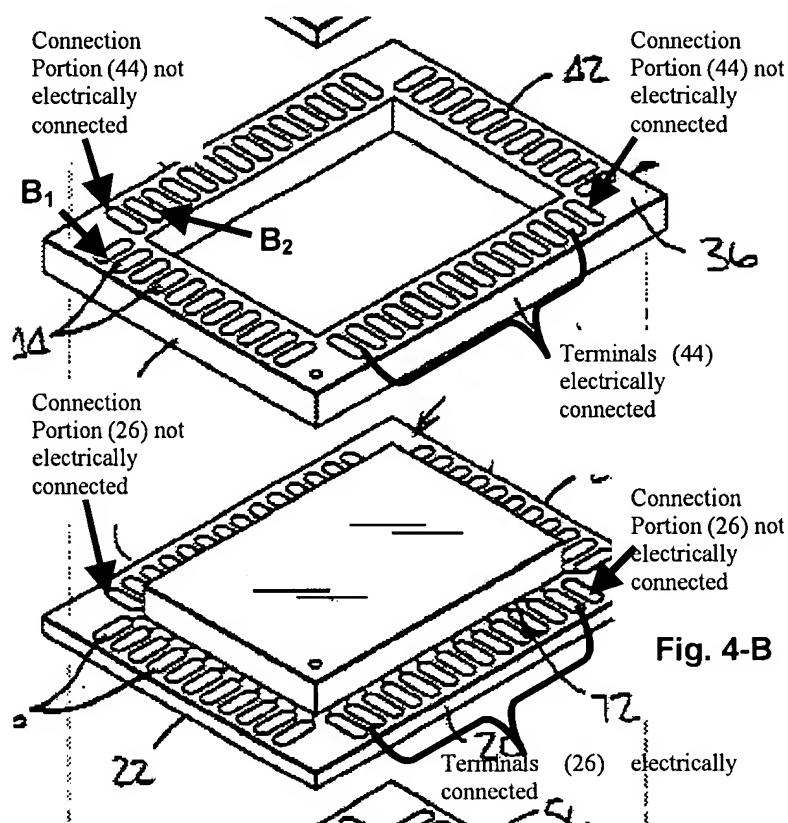
2. Claims 9-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Isaak (US Pat. No. 6,472,735 B2).

Regarding claim 9, Isaak teaches a semiconductor device comprising:

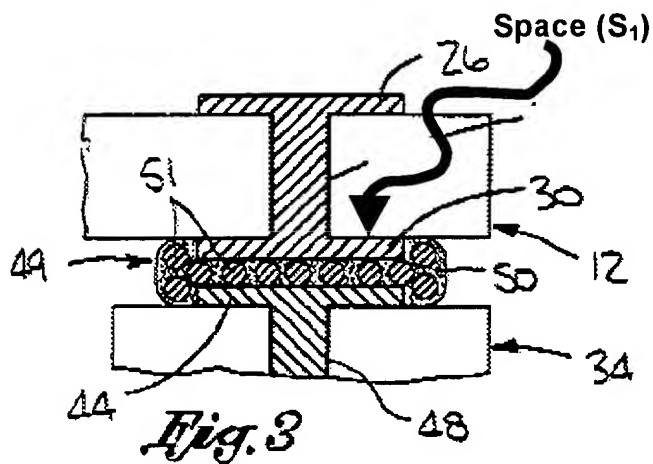
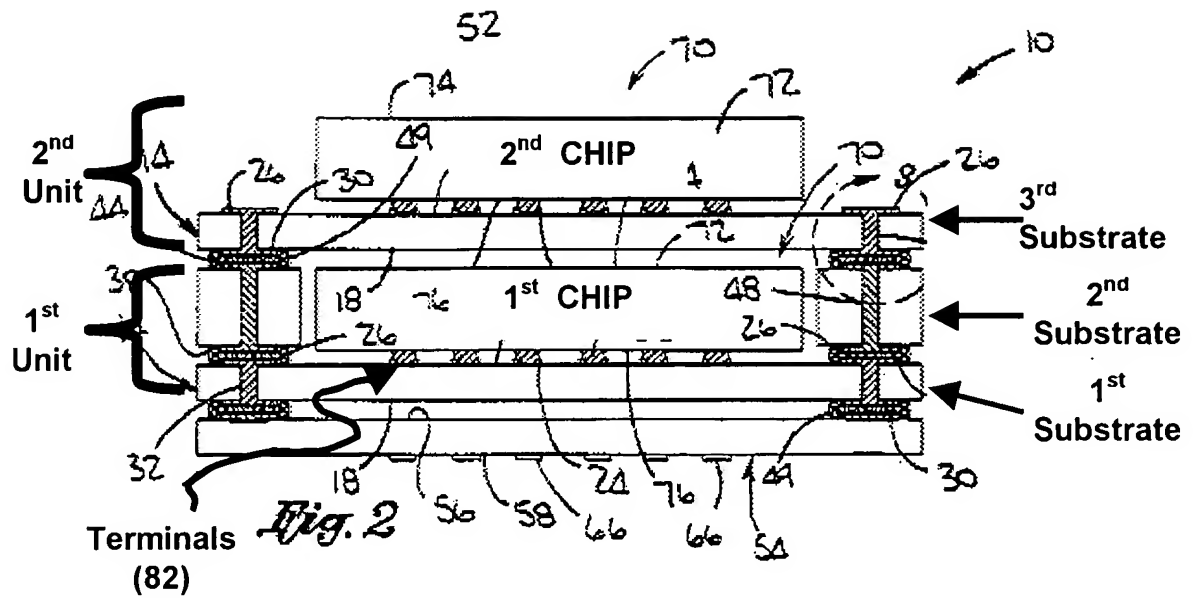
a first substrate (1<sup>st</sup> substrate 14) including an integrated circuit chip (1<sup>st</sup> chip 72) [See figures 2 and 4-A, attached below], first connection terminals electrically connected to terminals of the integrated circuit chip [consider the terminals 26 electrically connected to the chip 72 as shown in Figure 4-A, attached below], and a first connection portion spaced from the first connection terminals and not electrically connected to any terminal of the integrated circuit chip [consider Connection Portions 26 not electrically connected to the chip 72 as shown in Figure 4-A, attached below];



a second substrate (2<sup>nd</sup> substrate 34) stacked on the first substrate [see figures 2 and 4-B, attached below] and including second connection terminals [consider the terminals 44 electrically connected to the chip 72 as shown in Figure 4-B, attached below] and a second connection portion spaced from the second connection terminals [consider the Connection Portions 44 not electrically connected to the chip 72 as shown in Figure 4-B, attached below]; and



a metal material portion (30, 46, 51) provided between the first connection portion and the second connection portion [figures 2 and 3, attached below] and bonding the first connection portion to the second connection portion [figures 2 and 3, attached below] and not electrically connected to any terminal of the integrated circuit chip [consider the Connection Portions 26 and 44 not electrically connected to chip 72 in Figures 4-A and 4-B, attached above].



Regarding claim 10, Isaak further teaches a plurality of unit substrates (1<sup>st</sup> Unit and 2<sup>nd</sup> Unit as shown in fig. 2, attached above) that are stacked, each of the unit substrates being formed of the first (14) and second (34) substrates stacked (see fig. 2. and col. 8, lines 2-3. Please note that although it is not shown in the figures, Isaak, in col. 8, ll. 2-3, further teaches that an additional second substrate 34 can be provided on the 3<sup>rd</sup> substrate].

Regarding claim 11, Isaak further teaches an adhesive sheet (49,50) interposed between the unit substrates (1<sup>st</sup> Unit and 2<sup>nd</sup> Unit) adjacent each other a stacking direction and bonding the unit substrates together (see figs. 2 and 3, attached above).

Regarding claim 12, Isaak further teaches that the first connection portion is a first dummy terminal provided between the first connection terminals adjacent to each other in a plane direction [consider Connection Portion 26 located between terminals A<sub>1</sub> and A<sub>2</sub> as shown in Figure 4-A, attached above], and the second connection portion is a second dummy terminal provided between the second connection terminals adjacent to each other in the plane direction [consider Connection Portion 44 located between terminals B<sub>1</sub> and B<sub>2</sub> as shown in Figure 4-B, attached above].

Regarding claim 13, Isaak further teaches that the first connection portion is a first dummy pad provided on the first substrate (14) [consider Connection Portions 26 not electrically connected to the chip 72 as shown in Figure 4-A, attached above], and the second connection portion is a second dummy pad provided on the second substrate [consider the Connection Portions 44 not electrically connected to the chip 72 as shown in Figure 4-B, attached above].

Regarding claim 14, the court has held that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. See *In re Pearson* 181 USPQ 641 (CCPA 1974) and *In re Swinehart* 169 USPQ 226 (CCPA 1971). In the instance case, Isaak teaches connection portions (26) and (44), which are used to align substrates (12) and (34) [see figure 4]. Thus, Isaak anticipates the claimed invention since the prior art structure is capable of performing the intended use.

Regarding claim 15, Isaak further teaches that the metal material portion (30, 46) is formed of solder, tin, or an Sn-Bi alloy [col. 7, lines 58-61 and col. 8, lines 26-30].

Regarding claim 16, Isaak further teaches that the adhesive sheet (49, 50) is formed of resin [consider the epoxy material as disclosed in col. 61-63].

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 9-16 have been considered but are moot in view of the new ground of rejection. Please note that the claims are rejected in light of the new interpretation of figures 2-4 of Isaak.

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ohmori (US Pat. No. 6,492,718 B2) discloses a stacked



semiconductor device (see figs. 1 and 8); and Matsuo et al. (US 2002/0036338 A1) discloses a stacked semiconductor device (see fig. 1B).

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### ***Correspondence***

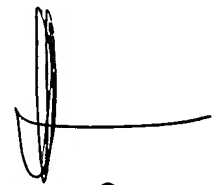
Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

José R. Díaz  
Examiner  
Art Unit 2815



SE Kenneth Parker  
TC2300